

WHAT IS CLAIMED IS:

- 1 1. A resistor comprising:
 - 2 a semiconductor layer;
 - 3 a body region formed in a portion of the semiconductor layer, the body region being
 - 4 doped to a first conductivity type and having a first resistivity;
 - 5 a first contact region formed in the semiconductor layer adjacent the body region, the first
 - 6 contact region being doped to the first conductivity type;
 - 7 a second contact region formed in the semiconductor layer spaced from the first contact
 - 8 region by the body region, the second contact region being doped to the first conductivity type;
 - 9 a dielectric layer overlying the body region, said dielectric comprising a material with a
 - 10 relative permittivity greater than about 8; and
 - 11 an electrode overlying said dielectric.
- 1 2. The resistor of claim 1 wherein the dielectric layer comprises a material selected from the
 - 2 group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium silicate,
 - 3 zirconium oxide, zirconium oxynitride, zirconium silicate, yttrium oxide, lanthanum oxide,
 - 4 cerium oxide, titanium oxide, tantalum oxide, and combinations thereof.
- 1 3. The resistor of claim 1 wherein the dielectric layer has a relative permittivity greater than
 - 2 about 10.
- 1 4. The resistor of claim 1 wherein the dielectric layer has a relative permittivity greater than
 - 2 about 20.

- 1 5. The resistor of claim 1 wherein the dielectric layer has a physical thickness greater than
2 about 5 angstroms.
- 1 6. The resistor of claim 1 wherein the dielectric layer has a physical thickness greater than
2 about 20 angstroms.
- 1 7. The resistor of claim 1 wherein the dielectric layer has a physical thickness greater than
2 about 40 angstroms.
- 1 8. The resistor of claim 1 wherein the semiconductor layer comprises a silicon layer.
- 1 9. The resistor of claim 1 wherein the semiconductor comprises silicon and germanium.
- 1 10. The resistor of claim 1 wherein the semiconductor layer has a thickness in the range of
2 about 20 angstroms to about 400 angstroms.
- 1 11. The resistor of claim 1 further comprising an insulator layer underlying the
2 semiconductor layer.
- 1 12. The resistor of claim 11 wherein the insulator layer comprises silicon oxide.
- 1 13. The resistor of claim 1 wherein the electrode comprises a semiconductor.
- 1 14. The resistor of claim 1 wherein the electrode comprises a metal selected from the group
2 consisting of molybdenum, tungsten, titanium, tantalum, platinum, and hafnium.

- 1 15. The resistor of claim 1 wherein the electrode comprises a metallic nitride selected from
2 the group consisting of molybdenum nitride, tungsten nitride, titanium nitride, and tantalum
3 nitride, and combinations thereof.
- 1 16. The resistor of claim 1 wherein the electrode comprises a metallic silicide selected from
2 the group consisting of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide,
3 tantalum silicide, platinum silicide, and erbium silicide, and combinations thereof.
- 1 17. The resistor of claim 1 wherein the electrode comprises a metallic oxide selected from the
2 group consisting of ruthenium oxide, and indium tin oxide, and combinations thereof.
- 1 18. The resistor of claim 1 wherein the electrode has a width larger than about 0.1 microns.
- 1 19. The resistor of claim 1 wherein the electrode has a width larger than about 1 micron.
- 1 20. The resistor of claim 1 wherein the electrode has a length larger than about 0.1 microns.
- 1 21. The resistor of claim 1 wherein the electrode has a length larger than about 1 micron.
- 1 22. The resistor of claim 1 wherein the first conductivity type is n-type.
- 1 23. The resistor of claim 1 wherein the first conductivity type is p-type.
- 1 24. The resistor of claim 1 further comprising spacers formed on sides of the electrode.
- 1 25. The resistor of claim 24 wherein the spacers comprise silicon nitride.

1 26. The resistor of claim 24 further comprising an etch-stop layer overlying the electrode and
2 the spacers.

1 27. The resistor of claim 26 wherein the etch-stop layer comprise silicon nitride.

1 28. A silicon-on-insulator resistor comprising:
2 a silicon layer overlying an insulator layer;
3 a body region formed in a portion of the silicon layer;
4 a dielectric layer overlying the body region, said dielectric comprising a high permittivity
5 dielectric layer;
6 a top electrode overlying said dielectric layer; and
7 a pair of doped regions formed in the silicon layer oppositely adjacent the body region,
8 the pair of doped regions being doped to the same conductivity type as the body region.

1 29. The resistor of claim 28 wherein the high permittivity dielectric is selected from a group
2 comprising of aluminum oxide, hafnium oxynitride, hafnium silicate, zirconium oxide,
3 zirconium oxynitride, zirconium silicate, yttrium oxide, lanthanum oxide, cerium oxide, titanium
4 oxide, and tantalum oxide, and combinations thereof.

1 30. The resistor of claim 28 wherein the permittivity dielectric layer comprises hafnium
2 oxide.

1 31. The resistor of claim 28 wherein the high permittivity dielectric has a relative permittivity
2 greater than about 8.

1 32. The resistor of claim 28 wherein the high permittivity dielectric has a relative permittivity
2 greater than about 10.

1 33. The resistor of claim 28 wherein the high permittivity dielectric has a relative permittivity
2 greater than about 20.

1 34. The resistor of claim 28 wherein the dielectric has a physical thickness greater than about
2 5 angstroms.

1 35. The resistor of claim 28 wherein the dielectric has a physical thickness greater than about
2 20 angstroms.

1 36. The resistor of claim 28 wherein the dielectric has a physical thickness greater than about
2 40 angstroms.

1 37. The resistor of claim 28 wherein the silicon layer is a strained silicon layer.

1 38. The resistor of claim 28 wherein the silicon layer has a thickness in the range of about 20
2 angstroms to about 1000 angstroms.

1 39. The resistor of claim 28 wherein the silicon layer has a thickness in the range of about 20
2 angstroms to about 400 angstroms.

1 40. The resistor of claim 28 wherein the insulator layer comprises silicon oxide.

1 41. The resistor of claim 28 wherein the electrode comprises polycrystalline silicon,
2 polycrystalline silicon-germanium, a metal, a metallic nitride, a metallic silicide, and a metallic
3 oxide, and combinations thereof.

1 42. The resistor of claim 41 wherein the metal is selected from the group consisting of
2 molybdenum, tungsten, titanium, tantalum, platinum, and hafnium.

1 43. The resistor of claim 41 wherein the metallic nitride is selected from the group consisting
2 of molybdenum nitride, tungsten nitride, titanium nitride, and tantalum nitride, and combinations
3 thereof.

1 44. The resistor of claim 41 wherein the metallic silicide is selected from the group
2 consisting of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, tantalum silicide,
3 platinum silicide, and erbium silicide, and combinations thereof.

1 45. The resistor of claim 28 wherein the electrode has a width greater than about 0.1 microns.

1 46. The resistor of claim 28 wherein the electrode has a width greater than about 1 micron.

1 47. The resistor of claim 28 wherein the electrode has a length greater than about 0.1
2 microns.

1 48. The resistor of claim 28 wherein the electrode has a length greater than about 1 micron.

1 49. The resistor of claim 28 wherein the body and the doped regions are doped n-type.

1 50. The resistor of claim 28 wherein the body and the doped regions are doped p-type.

1 51. The resistor of claim 28 further comprising spacers formed on sides of the electrode.

1 52. The resistor of claim 51 wherein the spacers comprise silicon nitride.

1 53. The resistor of claim 51 further comprising an etch-stop layer overlying the electrode and
2 the spacers.

- 1 54. The resistor of claim 53 wherein the etch-stop layer comprise silicon nitride.
- 1 55. The resistor of claim 54 further comprising an inter-layer dielectric overlying the etch-
2 stop layer.
- 1 56. The resistor of claim 55 wherein the inter-layer dielectric comprises silicon oxide.
- 1 57. The resistor of claim 55 further comprising a contact plug formed through the inter-layer
2 dielectric and in electrical contact with the resistor.
- 1 58. The resistor of claim 28 further comprising a shallow trench isolation region adjacent the
2 silicon layer.
- 1 59. The resistor of claim 28 wherein the resistor is formed in an active area of the silicon
2 layer and wherein the active area is isolated from other active areas that overlie the insulator
3 layer by mesa isolation.

1 60. A method of forming a resistor, the method comprising:
2 providing a silicon-on-insulator substrate that includes a silicon layer overlying an
3 insulator layer;
4 forming a resistor body of a first conductivity type in a portion of the silicon layer;
5 forming a dielectric layer overlying the body region, the dielectric layer comprising a
6 material with a relative permittivity greater than about 8;
7 forming a top electrode on the dielectric layer; and
8 forming a pair of doped regions of the first conductivity type oppositely adjacent the
9 body region.

1 61. The method of claim 60 wherein forming the resistor body comprises:
2 forming an active region;
3 forming isolation regions surrounding the active region; and
4 doping the active region.

1 62. The method of claim 61 wherein doping the active region employs an ion implantation
2 with a dose in the range of about 10^{13} to about 10^{16} cm^{-2} .

1 63. The method of claim 60 wherein forming the dielectric layer comprises a chemical vapor
2 deposition step.

1 64. The method of claim 60 wherein forming the dielectric layer comprises a sputtering
2 deposition step.

- 1 65. The method of claim 60 wherein forming the dielectric layer comprises:
2 forming an interfacial oxide layer; and
3 forming a high permittivity dielectric layer.
- 1 66. The method of claim 60 wherein forming the pair of doped regions comprises:
2 doping a portion of the silicon layer not covered by the top electrode;
3 forming spacers on sidewalls of the top electrode; and
4 doping a portion of the silicon layer not covered by the top electrode and the spacers.
- 1 67. The method of claim 66 wherein the spacers comprise silicon nitride.
- 1 68. The method of claim 66 further comprising:
2 depositing an etch-stop layer over the top electrode and the spacers;
3 forming an inter-layer dielectric over the etch-stop layer;
4 forming contact holes in the inter-layer dielectric layer; and
5 filling the contact holes with a conductive material to form contact plugs.
- 1 69. The method of claim 68 wherein the etch-stop layer comprises silicon nitride.
- 1 70. The method of claim 68 wherein the inter-layer dielectric comprises silicon oxide.
- 1 71. The method of claim 68 wherein a first contact plug electrically contacts one of the pair
2 of doped regions and a second contact plug electrically contacts the top electrode, said first and
3 second contact plugs being electrically connected.
- 1 72. The method of claim 60 wherein the insulator layer comprises silicon oxide.

- 1 73. The method of claim 60 wherein the insulator layer has a thickness of less than about
2 1200 angstroms.
- 1 74. The method of claim 60 wherein the silicon layer has a thickness in the range of about 20
2 angstroms to about 1000 angstroms.
- 1 75. The method of claim 60 wherein the top electrode comprises a semiconductor.
- 1 76. The method of claim 60 wherein the top electrode comprises a metal selected from the
2 group consisting of molybdenum, tungsten, titanium, tantalum, platinum, and hafnium.
- 1 77. The method of claim 60 wherein the top electrode comprises a metallic nitride selected
2 from the group consisting of molybdenum nitride, tungsten nitride, titanium nitride, tantalum
3 nitride, or combinations thereof.
- 1 78. The method of claim 60 wherein the top electrode comprises a metallic silicide selected
2 from the group consisting of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide,
3 tantalum silicide, platinum silicide, and erbium silicide, and combinations thereof.
- 1 79. The method of claim 60 wherein the top electrode comprises a metallic oxide selected
2 from the group comprising of ruthenium oxide, and indium tin oxide, and combinations thereof.
- 1 80. The method of claim 60 wherein the dielectric layer comprises a material selected from
2 the group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium silicate,
3 zirconium oxide, zirconium oxynitride, and zirconium silicate, and combinations thereof.

1 81. The method of claim 60 wherein the dielectric layer has a relative permittivity of larger
2 than about 10.

1 82. The method of claim 60 wherein the dielectric layer has a relative permittivity of larger
2 than about 20.

1 83. The method of claim 60 wherein the dielectric has a physical thickness greater than about
2 5 angstroms.

1 84. The method of claim 83 wherein the dielectric has a physical thickness greater than about
2 20 angstroms.

1 85. The method of claim 84 wherein the dielectric has a physical thickness greater than about
2 40 angstroms.

1 86. The method of claim 60 wherein the electrode has a width greater than about 0.1 microns.

1 87. The method of claim 60 wherein the electrode has a width greater than about 1 micron.

1 88. The method of claim 60 the electrode has a length greater than about 0.1 microns.

1 89. The method of claim 61 wherein the electrode has a length greater than about 1 micron.

1 90. A silicon-on-insulator device comprising:
2 an active area comprising a silicon layer overlying an insulator layer;
3 a body region of a first conductivity type formed in a portion of the silicon layer;
4 a dielectric layer overlying the body region, said dielectric comprising a material selected
5 from the group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium
6 silicate, zirconium oxide, zirconium oxynitride, zirconium silicate, yttrium oxide, lanthanum
7 oxide, cerium oxide, titanium oxide, tantalum oxide, and combinations thereof;
8 a top electrode overlying the dielectric layer; and
9 a pair of doped regions of the first conductivity type formed in the silicon layer
10 oppositely adjacent the body region.

1 91. The device of claim 90 wherein the dielectric layer comprises hafnium oxide.

1 92. The device of claim 90 wherein the silicon layer has a thickness in the range of about 20
2 angstroms to about 400 angstroms.

1 93. The device of claim 90 and further comprising a second active area overlying the
2 insulator layer, the second active area including a transistor formed therein.

1 94. The device of claim 93 wherein the transistor includes a gate dielectric formed of the
2 same material as the dielectric layer overlying the body region.

1 95. The device of claim 93 wherein the transistor includes a gate dielectric formed of a
2 different material as the dielectric layer overlying the body region.

1 96. The device of claim 93 wherein the transistor includes a gate electrode formed of the
2 same material as the top electrode.

1 97. The device of claim 90 and further comprising an interfacial layer overlying and abutting
2 the body region, the dielectric layer overlying the interfacial layer.

1 98. The device of claim 97 wherein the interfacial layer comprises silicon oxide or silicon
2 oxynitride.

1 99. A silicon-on-insulator device comprising:
2 a substrate;
3 an insulator layer overlying the substrate;
4 an active area formed in a silicon layer overlying the insulator layer;
5 a body region of a first conductivity type formed in a portion of the silicon layer;
6 an interfacial layer overlying and abutting the body region;
7 a high-k dielectric layer overlying the interfacial layer, the high-k dielectric layer
8 comprising a material having a relative permittivity greater than about 8;
9 a top electrode overlying the high-k dielectric layer; and
10 a pair of doped regions of the first conductivity type formed in the active area oppositely
11 adjacent the body region.

1 100. The device of claim 99 wherein the high-k dielectric comprises a material selected from
2 the group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium silicate,
3 zirconium oxide, zirconium oxynitride, zirconium silicate, yttrium oxide, lanthanum oxide,
4 cerium oxide, titanium oxide, tantalum oxide, and combinations thereof.

1 101. The device of claim 100 wherein the dielectric layer comprises hafnium oxide.

1 102. The device of claim 100 and further comprising a second active area overlying the
2 insulator layer, the second active area including a transistor formed therein.

1 103. The device of claim 102 wherein the transistor includes a gate dielectric comprising a
2 material having a relative permittivity greater than about 8.

1 104. The device of claim 103 wherein the gate dielectric and the high-k dielectric comprise the
2 same material.

1 105. The device of claim 102 wherein the transistor includes a gate electrode formed of the
2 same material as the top electrode.

1 106. The device of claim 99 wherein the interfacial layer comprises silicon oxide.

1 107. The device of claim 99 wherein the interfacial layer comprises silicon oxynitride.

1 108. An electrostatic discharge protection circuit comprising:
2 an I/O pad;
3 a circuit that is to be protected;
4 a diode coupled between the I/O pad and a reference voltage node;
5 a resistor coupled between the I/O pad and the circuit, the resistor including a body
6 region, a first contact region adjacent the body region to electrically couple the body region to
7 the I/O pad, a second contact region adjacent the body region to electrically couple the body
8 region to the circuit, a dielectric layer having a relative permittivity greater than about 8
9 overlying the body region, and an electrode overlying the dielectric layer.

1 109. The circuit of claim 108 wherein the diode comprises:
2 a diode body region;
3 a diode dielectric having a relative permittivity greater than about 8 overlying the diode
4 body region;

5 a diode electrode overlying the diode dielectric; and
6 a p-doped region and an n-doped region oppositely adjacent to the diode body region.

1 110. The circuit of claim 109 wherein the p-doped region of the diode is electrically coupled
2 to the I/O pad and the n-doped region of the diode is electrically coupled to the reference voltage
3 node.

1 111. The circuit of claim 109 wherein the n-doped region of the diode is electrically coupled
2 to the I/O pad and the p-doped region of the diode is electrically coupled to the reference voltage
3 node.

1 112. The circuit of claim 108 and further comprising a second diode coupled between the I/O
2 pad and a second reference voltage node.

1 113. The circuit of claim 112 wherein the second diode comprises:
2 a diode body region;
3 a diode dielectric having a relative permittivity greater than about 8 overlying the diode
4 body region;
5 a diode electrode overlying the diode dielectric; and
6 a p-doped region and an n-doped region oppositely adjacent to the diode body region.

1 114. The circuit of claim 112 and further comprising:
2 a second circuit; and
3 a second resistor coupled between the second circuit and the I/O pad, the second resistor
4 comprising a body region, a first contact region adjacent the body region to electrically couple

5 the body region to the I/O pad, a second contact region adjacent the body region to electrically
6 couple the body region to the second circuit, a dielectric layer having a relative permittivity
7 greater than about 8 overlying the body region, and an electrode overlying the dielectric layer.

1 115. The circuit of claim 114 wherein the circuit comprises an output circuit and wherein the
2 second circuit comprises an input circuit.